

## **ABSTRACT OF THE DISCLOSURE**

Disclosed herein are an SRAM-compatible memory and method of driving the SRAM-compatible memory. The SRAM-compatible memory has memory banks, a parity generator and a parity bank. The memory banks each store corresponding one of input data in its DRAM cells specified by an input address. The memory banks perform write operations independently such that when a refresh operation or a write operation for a previous frame is being performed with respect to DRAM cells of a certain memory bank, the write operation of the input data is independently performed with respect to the respective memory banks except for the certain memory bank.

10 The parity generator generates a input parity determined based on the input data and a certain preset parity value. The parity bank stores the input parity.